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Assistant Commissioner for Patents
Washington, D.C. 20231

On 3/22/02

TOWNSEND and TOWNSEND and CREW LLP

By: [signature]

PATENT
Attorney Docket No.: 00939H-081300US
Client Ref. No.: P00H9023/US/kj

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

HAN, JONG-HEE

Application: No. 09/742,816

Filed: 12/19/2000

For: DELAY LOCKED LOOP FOR USE IN SEMICONDUCTOR MEMORY DEVICE

Examiner: Hoai V. Ho

Art Unit: 2818

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed December 26, 2001, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please replace the indicated paragraphs as follows:

Paragraph beginning at page 1, line 24 through page 2, line 5:

The delayed clock signal Delayed_clock is fed to a pre-delay/post-delay comparison block 110 that compares the delayed clock signal Delayed_clock with a reference clock signal Reference_clock to thereby determine whether increasing or decreasing the predetermined delay time is required. Through the comparison process,

A'